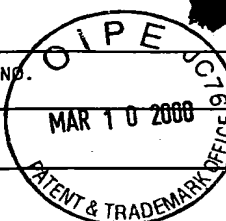


FORM PTO-1449

INFORMATION DISCLOSURE STATEMENT

ATTY. DOCKET NO.
SP035.C5APPLICANT
Garg *et al.*FILING DATE
June 10, 1999APPLICATION NO.
09/329,354GROUP
2763

RECEIVED
MAR 13 2000
Group 2763

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	PENDING DATE
<i>W</i>	AA1	4,626,989	12/1986	Torii	364	200	
	AB1	4,675,806	06/1987	Uchida	364	200	
	AC1	4,722,049	01/1988	Lahti	364	200	
	AD1	4,807,115	02/1989	Torng	364	200	
	AE1	4,901,233	02/1990	Liptay	395	375	
	AF1	4,903,196	02/1990	Pomerene <i>et al.</i>	364	200	
	AG1	4,942,525	07/1990	Shintani <i>et al.</i>	395	375	
	AH1	4,992,938	02/1991	Cocke <i>et al.</i>	364	200	
<i>W</i>	AI1	5,067,069	11/1991	Fite <i>et al.</i>	395	375	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
<i>W</i>	AJ1	O 515 166	11/1992	EP			Yes No
<i>W</i>	AK1	O 533 337	03/1993	EP			Yes No
<i>W</i>	AL1	WO 91/20031	12/1991	PCT			Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

<i>W</i>	AM	1	Acosta, Ramón D. <i>et al.</i> , "An Instruction Issuing Approach to Enhancing Performance in Multiple Functional Unit Processors," <i>IEEE Transactions On Computers</i> , Vol. C-35, No. 9, September 1986, pp. 815-828.
<i>W</i>	AN	1	Agerwala <i>et al.</i> , "High Performance Reduced Instruction Set Processors," IBM Research Division, March 31, 1987, pp. 1-61.
<i>W</i>	AO	1	Aiken, A. and Nicolau, A., "Perfect Pipelining: A New Loop Parallelization Technique*," pp. 221-235.
<i>W</i>	AR	1	Butler, M. and Patt, Y., "An Improved Area-Efficient Register Alias Table for Implementing HPS," University of Michigan, Ann Arbor, Michigan, January 1990, pp. 1-15.
<i>W</i>	AS	1	Butler, M. <i>et al.</i> , "Single Instruction Stream Parallelism Is Greater Than Two," <i>Proceedings of ISCA-18</i> , May 1990, pp. 276-286.

EXAMINER

LARRY D. DONAGHUE
PRIMARY EXAMINER

DATE CONSIDERED

03/22/00

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.



FORM PTO-1449

INFORMATION DISCLOSURE STATEMENT

ATTY. DOCKET NO.
SP035.C5APPLICATION NO.
09/329,354APPLICANT
Garg *et al.*FILING DATE
June 10, 1999GROUP
2763

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
<i>J</i>	AA2	5,109,495	04/1992	Fite <i>et al.</i>	395	375	
	AB2	5,142,633	08/1992	Murray <i>et al.</i>	395	375	
	AC2	5,214,763	05/1993	Blaner <i>et al.</i>	395	375	
	AD2	5,222,244	06/1993	Carbine <i>et al.</i>	395	800	
	AE2	5,226,126	07/1993	McFarland <i>et al.</i>	395	375	
	AF2	5,230,068	07/1993	Van Dyke <i>et al.</i>	395	375	
	AG2	5,251,306	10/1993	Tran	395	375	
	AH2	5,261,071	11/1993	Lyon	395	425	
<i>S</i>	AI2	5,345,569	09/1994	Tran	395	375	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ2						Yes No
	AK2						Yes No
	AL2						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

<i>l</i>	AM	<u>2</u>	Charlesworth, A.E., "An Approach to Scientific Array Processing: The Architectural Design of the AP-120B/FPS-164 Family," <i>Computer</i> , Vol. 14, September 1981, pp. 18-27.
<i>h</i>	AN	<u>2</u>	Colwell <i>et al.</i> , "A VLIW Architecture for a Trace Scheduling Compiler," <i>Proceedings of the 2nd International Conference on Architectural Support for Programming Languages and Operating Systems</i> , October 1987, pp. 180-192.
<i>ny</i>	AO	<u>2</u>	Dwyer, "A Multiple, Out-of-Order, Instruction Issuing System For Superscaler Processors," (All); Aug. 1991.
<i>W</i>	AR	<u>2</u>	Foster <i>et al.</i> , "Percolation of Code to Enhance Parallel Dispatching and Execution," <i>IEEE Trans. On Computers</i> , December 1971, pp. 1411-1415.
<i>W</i>	AS	<u>2</u>	Gee, J. <i>et al.</i> , "The Implementation of Prolog via VAX 8600 Microcode," <i>Proceedings of Micro 19</i> , New York City, October 1986, pp. 1-7.

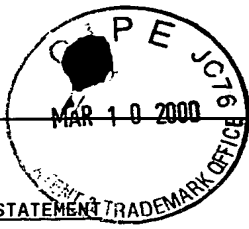
EXAMINER

LARRY D. DONAGHUE
PRIMARY EXAMINER

DATE CONSIDERED

05/27/00

EXAMINER: Initial if reference is considered pertinent or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.



FORM PTO-1449

INFORMATION DISCLOSURE STATEMENT

ATTY. DOCKET NO.
SP035.C5APPLICATION NO.
09/329,354APPLICANT
Garg *et al.*FILING DATE
June 10, 1999GROUP
2763

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	LINE DATE
<i>g</i>	AA3	5,355,457	10/1994	Shebanow <i>et al.</i>	395	375	
	AB3	5,398,330	03/1995	Johnson	395	375	
	AC3	5,442,757	08/1995	McFarland <i>et al.</i>	395	375	
	AD3	5,448,705	09/1995	Nguyen <i>et al.</i>	395	375	
	AE3	5,487,156	01/1996	Popescu <i>et al.</i>	395	375	
	AF3	5,497,499	03/1996	Garg <i>et al.</i>	395	800.73	
	AG3	5,561,776	10/1996	Popescu <i>et al.</i>	395	375	
	AH3	5,574,927	11/1996	Scantlin	395	800	
<i>g</i>	AI3	5,592,636	01/1997	Popescu <i>et al.</i>	395	586	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ3						Yes No
	AK3						Yes No
	AL3						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

<i>u</i>	AM	3	Goodman, J.R. and Hsu, W., "Code Scheduling and Register Allocation in Large Basic Blocks," <i>ACM</i> , 1988, pp. 442-452.
<i>7</i>	AN	3	Gross <i>et al.</i> , "Optimizing Delayed Branches," <i>Proceedings of the 5th Annual Workshop on Microprogramming</i> , October 5-7, 1982, pp. 114-120.
<i>u</i>	AO	3	Groves, R.D. and Oehler, R., "An IBM Second Generation RISC Processor Architecture," <i>IEEE</i> , 1989, pp. 134-137.
<i>u</i>	AR	3	Hennessy, J.L. and Patterson, D.A., <i>Computer Architecture A Quantitative Approach</i> , 1990, Ch. 6.4, 6.7 and pg. 449.
<i>u</i>	AS	3	Horst, R.W. <i>et al.</i> , "Multiple Instruction Issue in the NonStop Cyclone Processor," <i>IEEE</i> , 1990, pp. 216-226.

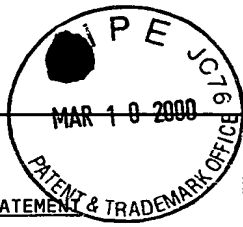
EXAMINER

LARRY D. DONAGHUE
PRIMARY EXAMINER

DATE CONSIDERED

03/22/01

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.



FORM PTO-1449

INFORMATION DISCLOSURE STATEMENT

ATTY. DOCKET NO.
SP035.C5APPLICATION NO.
09/329,354APPLICANT
Garg et al.FILING DATE
June 10, 1999GROUP
2763

RECEIVED
MAR 15 2000
Group 2763

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA4	5,625,837	04/1997	Popescu et al.	395	800	
	AB4	5,627,983	05/1997	Popescu et al.	395	393	
	AC4	5,708,841	01/1998	Popescu et al.	355	800	
	AD4	5,737,624	04/1998	Garg et al.	395	800.73	
	AE4	5,768,575	06/1998	McFarland et al.	395	569	
	AF4	5,778,210	07/1998	Henstrom et al.	395	394	
	AG4	5,797,025	08/1998	Popescu et al.	395	800	
	AH4	5,832,205	11/1998	Kelly et al.	395	185.06	
	AI4	5,832,293	11/1998	Popescu et al.	395	800.23	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ4						Yes No
	AK4						Yes No
	AL4						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AM	4	Hwu, W. et al., "An HPS Implementation of VAX: Initial Design and Analysis," <i>Proceedings of the Nineteenth Annual Hawaii International Conference on System Sciences</i> , 1986, pp. 282-291.
	AN	4	Hwu, W. et al., "Checkpoint Repair for High-Performance Out-of-Order Execution Machines," <i>IEEE Trans. On Computers</i> , Vol. C-36, No. 12, December 1987, pp. 1496-1514.
	AO	4	Hwu, W. and Patt, Y.N., "Design Choices for the HPSm Microprocessor Chip," <i>Proceedings of the Twentieth Annual Hawaii International Conference on System Sciences</i> , 1987, pp. 330-336, 1987.
	AR	4	Hwu, W. et al., "Experiments with HPS, a Restricted Data Flow Microarchitecture for High Performance Computers," <i>COMPCON 86</i> , 1986.
	AS	4	Hwu, W. et al., "Exploiting Parallel Microprocessor Microarchitectures with a Compiler Code Generator," <i>Proceedings of the 15th Annual Symposium on Computer Architecture</i> , June 1988, pp. 45-53.

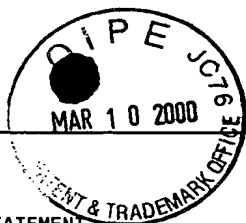
EXAMINER

LARRY D. DONAGHUE
PRIMARY EXAMINER

DATE CONSIDERED

03/22/00

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

FORM PTO-1449
INFORMATION DISCLOSURE STATEMENTATTY. DOCKET NO.
SP035.C5APPLICATION NO.
09/329,354APPLICANT
Garg et al.FILING DATE
June 10, 1999GROUP
2763RECEIVED
MAR 13 2000
Group 2763






U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA5						
	AB5						
	AC5						
	AD5						
	AE5						
	AF5						
	AG5						
	AH5						
	AI5						

FOREIGN PATENT DOCUMENTS

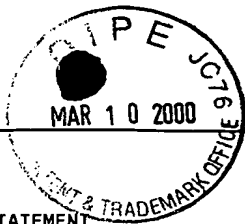
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ5						Yes No
	AK5						Yes No
	AL5						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AM	5	Hwu, W. and Patt, Y.N., "HPSm, a High Performance Restricted Data Flow Architecture Having Minimal Functionality," <i>Proceedings of the 18th International Symposium on Computer Architecture</i> , pp. 297-306, June 1986.
	AN	5	Hwu, W. and Patt, Y.N., "HPSm2: A Refined Single-chip Microengine," <i>HICSS '88</i> , 1988, pp. 30-40.
	AO	5	Johnson, William M., <u>Super-Scalar Processor Design</u> , (Dissertation), Copyright 1989, 134 pages.
	AR	5	Jouppi et al., "Available Instruction-Level Parallelism for Superscalar and Superpipelined Machines," <i>Proceedings of the 3rd International Conference on Architectural Support for Programming Languages and Operating Systems</i> , April 1989, pp. 272-282.
	AS	5	Jouppi, N.H., "Integration and Packaging Plateaus of Processor Performance," <i>IEEE</i> , 1989, pp. 229-232.

EXAMINER
LARRY D. DONAGHUE
PRIMARY EXAMINERDATE CONSIDERED
03/22/00

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

FORM PTO-1449
INFORMATION DISCLOSURE STATEMENTATTY. DOCKET NO.
SP035.C5APPLICATION NO.
09/329,354APPLICANT
Garg *et al.*FILING DATE
June 10, 1999GROUP
2763RECEIVED
MAR 13 2000
Group 2763

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA6						
	AB6						
	AC6						
	AD6						
	AE6						
	AF6						
	AG6						
	AH6						
	AI6						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ6						Yes No
	AK6						Yes No
	AL6						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

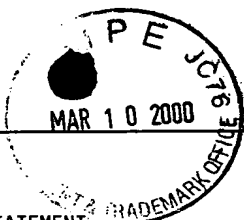
	AM	<u>6</u>	Jouppi, N.P., "The Nonuniform Distribution of Instruction-Level and Machine Parallelism and Its Effect on Performance," <i>IEEE Transactions on Computers</i> , Vol. 38, No. 12, December 1989, pp. 1645-1658.
	AN	<u>6</u>	Keller, "Look-Ahead Processors"; Dec. 1975, pp. 177-194.
	AO	<u>6</u>	Lam, M.S., "Instruction Scheduling For Superscalar Architectures," <i>Annu. Rev. Comput. Sci.</i> , Vol. 4, 1990, pp. 173-201.
	AR	<u>6</u>	Lightner <i>et al.</i> , "The Metaflow Architecture", <i>IEEE Micro Magazine</i> , June 1991, pp. 11-12 and 63-68.
	AS	<u>6</u>	Lightner <i>et al.</i> , "The Metaflow Lightning" Chip Set Mar. 1991 <i>IEEE Lightning Outlined. Microprocessor Report</i> , September 1990.

EXAMINER

DATE CONSIDERED

03/27/00

EXAMINER: Initial if reference is ~~not~~ known, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.



FORM PTO-1449

INFORMATION DISCLOSURE STATEMENT

ATTY. DOCKET NO.
SP035.C5APPLICATION NO.
09/329,354

MAR 13 2000

APPLICANT
Garg et al.FILING DATE
June 10, 1999GROUP
2763

Group 2700

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA7						
	AB7						
	AC7						
	AD7						
	AE7						
	AF7						
	AG7						
	AH7						
	AI7						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ7						Yes No
	AK7						Yes No
	AL7						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

M	AM	Z	Melvin, S. and Patt, Y., "Exploiting Fine-Grained Parallelism Through a Combination of Hardware and Software Techniques," <i>Proceedings From ISCA-18</i> , May 1990, pp. 287-296.
M	AN	Z	Murakami, K. et al., "SIMP (Single Instruction stream/Multiple instruction Pipelining): A Novel High-Speed Single-Processor Architecture," <i>ACM</i> , 1989, pp. 78-85.
M	AO	Z	Patt, Y.N. et al., "Critical Issues Regarding HPS, A High Performance Microarchitecture," <i>The 18th Annual Workshop on Microprogramming</i> , Pacific Grove, California, Dec. 3-6, 1985, IEEE Computer Order No. 653, pp. 109-116.
M	AR	Z	Patt, Y.N. et al., "HPS, A New Microarchitecture: Rationale and Introduction," <i>The 18th Annual Workshop on Microprogramming</i> , Pacific Grove, California, Dec. 3-6, 1985; IEEE Computer Society Order No. 653, pp. 103-108.
M	AS	Z	Patt, Y.N. et al., "Run-Time Generation of HPS Microinstructions From a VAX Instruction Stream," <i>Proceedings of MICRO 19 Workshop</i> , New York, New York, October 1986, pp. 1-7.

EXAMINER

LARRY D. DONAGHUE
PRIMARY EXAMINER

DATE CONSIDERED

03/22/00

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.



FORM PTO-1449

INFORMATION DISCLOSURE STATEMENT

ATTY. DOCKET NO.
SP035.C5APPLICATION NO.
09/329,354APPLICANT
Garg *et al.*FILING DATE
June 10, 1999GROUP
2763

MAR 13 2000

Group 2700

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA8						
	AB8						
	AC8						
	AD8						
	AE8						
	AF8						
	AG8						
	AH8						
	AI8						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ8						Yes No
	AK8						Yes No
	AL8						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AM	<u>8</u>	Peleg <i>et al.</i> , "Future Trends in Microprocessors: Out-Of-Order Execution, Spec. Branching and Their CISC Performance Potential", March 1991.
	AN	<u>8</u>	Pleszkun <i>et al.</i> , "The Performance Potential of Multiple Functional Unit Processors," <i>Proceedings of the 15th Annual Symposium on Computer Architecture</i> , June 1988, pp. 37-44.
	AO	<u>8</u>	Pleszkun <i>et al.</i> , "WISQ: A Restartable Architecture Using Queues," <i>Proceedings of the 14th International Symposium on Computer Architecture</i> , June 1987, pp. 290-299.
	AR	<u>8</u>	Smith, M.D. <i>et al.</i> , "Boosting Beyond Static Scheduling in a Superscalar Processor," <i>IEEE</i> , 1990, pp. 344-354.
	AS	<u>8</u>	Smith <i>et al.</i> , "Implementation of Precise Interrupts in Pipelined Processors," <i>Proceedings of the 12th Annual International Symposium on Computer Architecture</i> , June 1985, pp. 36-44.

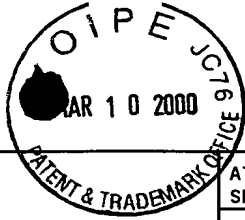
EXAMINER

LARRY D. DONAGHUE
PRIMARY EXAMINER

DATE CONSIDERED

03/22/00

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.



FORM PTO-1449

INFORMATION DISCLOSURE STATEMENT

ATTY. DOCKET NO.
SP035.C5APPLICATION NO.
09/329,354APPLICANT
Garg *et al.*FILING DATE
June 10, 1999GROUP
2763

RECEIVED

MAR 15 2000

U.S. PATENT DOCUMENTS

Group 2700

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA9						
	AB9						
	AC9						
	AD9						
	AE9						
	AF9						
	AG9						
	AH9						
	AI9						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ9						Yes No
	AK9						Yes No
	AL9						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AM	2	Smith, M.D. <i>et al.</i> , "Limits on Multiple Instruction Issue," <i>Computer Architecture News</i> , No. 2, April 17, 1989, pp. 290-302.
	AN	2	Sohi, G.S. <i>et al.</i> , "Instruction Issue Logic for High Performance, Interruptable Pipelined Processors," <i>The 14th Annual International Symposium on Computer Architecture</i> , June 2-5, 1987, pp. 27-34.
	AO	2	Swenson, J.A. and Patt, Y.N., "Hierarchical Registers for Scientific Computers," <i>St. Malo '88</i> , University of California at Berkeley, 1988, pp. 346-353.
	AR	2	Thornton, J.E., <u>Design of a Computer: The Control Data 6600</u> , Control Data Corporation, 1970, pp. 58-140.
	AS	2	Tjaden <i>et al.</i> , "Detection and Parallel Execution of Independent Instructions," <i>IEEE Trans. On Computers</i> , Vol. C-19, No. 10, October 1970, pp. 889-895.

EXAMINER

LARRY D. DONAGHUE
PRIMARY EXAMINER

DATE CONSIDERED

03/22/00

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.



FORM PTO-1449

INFORMATION DISCLOSURE STATEMENT

ATTY. DOCKET NO.
SP035.C5APPLICATION NO.
09/329,354APPLICANT
Garg *et al.*FILING DATE
June 10, 1999GROUP
2763






U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA10						
	AB10						
	AC10						
	AD10						
	AE10						
	AF10						
	AG10						
	AH10						
	AI10						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ10						Yes No
	AK10						Yes No
	AL10						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AM	<u>10</u>	Tjaden <i>et al.</i> , "Representation of Concurrency with Ordering Matrices," <i>IEEE Trans. On Computers</i> , Vol. C-22, No. 8, August 1973, pp. 752-761.
	AN	<u>10</u>	Tjaden, <u>Representation and Detection of Concurrency Using Ordering Matrices</u> , (Dissertation), 1972, pp. 1-199.
	AO	<u>10</u>	Tomasulo, R.M., "An Efficient Algorithm for Exploiting Multiple Arithmetic Units," <i>IBM Journal</i> , Vol. 11, January 1967, pp. 25-33.
	AR	<u>10</u>	Uht, A.K., "An Efficient Hardware Algorithm to Extract Concurrency From General-Purpose Code," <i>Proceedings of the 19th Annual Hawaii International Conference on System Sciences</i> , 1986, pp. 41-50.
	AS	<u>10</u>	Uvieghara, G.A. <i>et al.</i> , "An Experimental Single-Chip Data Flow CPU," <i>IEEE Journal of Solid-State Circuits</i> , Vol. 27, No. 1, January 1992, pp. 17-28.

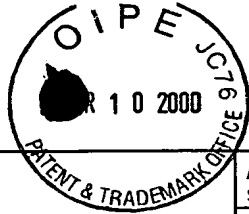
EXAMINER

LARRY D. DONAGHIE
PRIOR ART

DATE CONSIDERED

63/22/00

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.



FORM PTO-1449

INFORMATION DISCLOSURE STATEMENT

ATTY. DOCKET NO.
SP035.C5APPLICATION NO.
09/329,354APPLICANT
Garg *et al.*FILING DATE
June 10, 1999GROUP
2763RECEIVED
MAR 13 2000
Group 2700






U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA11						
	AB11						
	AC11						
	AD11						
	AE11						
	AF11						
	AG11						
	AH11						
	AI11						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ11						Yes No
	AK11						Yes No
	AL11						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AM	<u>11</u>	Uviegbara, G.A. <i>et al.</i> , "An Experimental Single-Chip Data Flow CPU," <i>Symposium on ULSI Circuits Design Digest of Technical Papers</i> , May 1990.
	AN	<u>11</u>	Wedig, R.G., <u>Detection of Concurrency In Directly Executed Language Instruction Streams</u> , (Dissertation), June 1982, pp. 1-179.
	AO	<u>11</u>	Weiss <i>et al.</i> , "Instruction Issue Logic in Pipelined Supercomputers," Reprinted from <i>IEEE Trans. on Computers</i> , Vol. C-33, No. 11, November 1984, pp. 1013-1022.
	AR	<u>11</u>	Wilson, J.E. <i>et al.</i> , "On Turning the Microarchitecture of an HPS Implementation of the VAX," <i>Proceedings of Micro 20</i> , December 1987, pp. 162-167.
	AS	<u>11</u>	<i>IBM Journal of Research and Development</i> , Vol. 34, No. 1, January 1990, pp. 1-70.

EXAMINER

LARRY D. DONAGHUE
PRIMARY EXAMINER

DATE CONSIDERED

03/32/00

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.